SINGLE OTRA BASED PD CONTROLLERS

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Abstract:
This paper presents a single Operational transresistance (OTRA) based voltage-mode proportional-derivative (PD) controller with independent tuning of proportional (Kp) and derivative (Kd) constants. This configuration can be made fully integrated by implementing the resistors using matched transistors operating in linear region. In order to verify the proposed circuit a closed loop control system using the proposed PD controller is designed and simulated using SPICE.

Key Words: OTRA, MOS implementation of a linear resistance, PD Controller, Second order LPF.

1. Introduction

The derivative (D) controllers with adjustable parameters are used to control integrating systems and systems with inertia. In either situation, pure derivative control is not used, for it is too fragile. Instead, proportional and derivative controls are mixed together to maximize the stability. Motor control and robot manipulators are examples of PD controllers.

Literature survey reveals that number of circuits have been reported relating to proportional (P), proportional integral (PI), proportional derivative (PD), and proportional integral & derivative (PID) controllers [1]–[7]. Circuits presented in [1],[2] are based on op-amps and have their own limitation of finite gain bandwidth.

Reference [3] presents OTA based controllers and [4] presents CDBA based controllers whereas CCII based controllers are proposed in [5]-[7]. In this paper an OTRA based controllers has been presented.

It is well known that inherent wide bandwidth which is virtually independent of closed loop gain, greater linearity, and large dynamic range is the key performance features of current mode technique [8]. Operational Transresistance Amplifier (OTRA) is a high gain current input, voltage output amplifier [9]. OTRA, being a current processing analog building block, inherits all the advantages of current mode technique. It is also free from parasitic input capacitances and resistances as its input terminals are virtually grounded and hence, non-ideality problem is less in circuits implemented using OTRA. Several high performance CMOS OTRA topologies have been proposed in literature [9]-[12] leading to growing interest in OTRA based analog signal processing circuits. In recent past OTRA has been extensively used as an analog building block for realizing a number of signal processing circuits such as filters[13]-[16], oscillators[17]-[19], multivibrators [20],[21] and immittance simulation circuits[17],[22]-[24].

This paper aims at presenting a PD controller using single OTRA two resistors and a capacitor having orthogonally tunable proportional and derivative constants. These circuits can be made fully integrated by implementing the resistors using MOS transistors operating in non-saturation region.

2. Circuit Description

2.1. *PD controller*

In PD controller as shown in Fig.1, the actuating signal, a(t) is sum of proportional to the error signal, e(t) and the derivative of e(t). Representing in s-domain can be written as

$$G_c(s) = K_p + K_d\, s \tag{1}$$

where KP and Kd are the proportional and derivative constants, respectively.(1) can alternatively be represented as

$$G_c(s) = K_p(1 + T_d\, s) \tag{2}$$

where Td=Kd / Kp. The amplitude M(ω) and phase Φ(ω) characteristics of (2) are given by

$$M(\omega) = K_p\sqrt{1 + (\omega T_d)^2} \tag{3}$$

$$\Phi(\omega) = \operatorname{arctg}(\omega T_d) \tag{4}$$

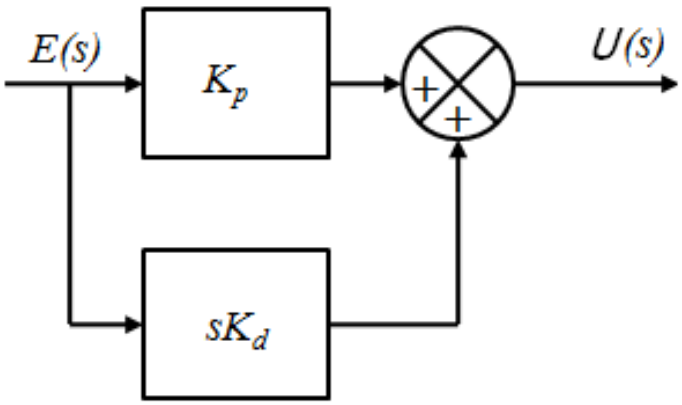

Fig. 1.Block Diagram of PD Controller

2.2. *OTRA based PD controller*

OTRA is a three terminal device [10] shown symbolically in Fig.2 and its port relations can be characterized by matrix (5).

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix} \tag{5}$$

For ideal operations the transresistance gain Rm approaches infinity and forces the input currents to be equal. Thus OTRA must be used in a negative feedback configuration [9],[10].

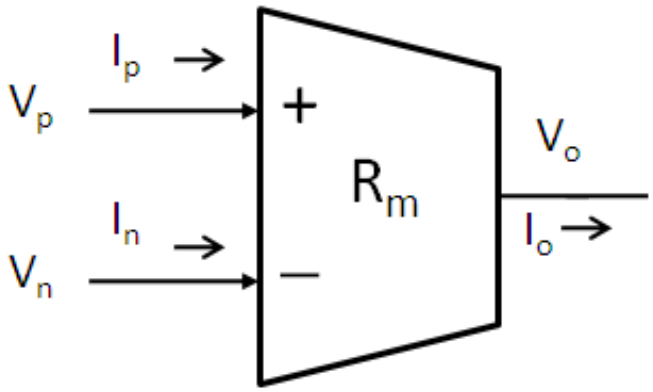

Fig. 2.OTRA Symbol

Proposed PD controller is shown in Fig. 3. The routine analysis of this controller gives the following voltage transfer function

$$\frac{V_o}{V_i} = \frac{R_f}{R} + sCR_f \tag{6}$$

And results in

$$K_p = \frac{R_f}{R} \quad K_d = CR_f \tag{7}$$

From the above equation it is clear that by varying R, Kp value can be adjusted independent of Kd and by simultaneous variation of Rf and R, Kd can be independently controlled.

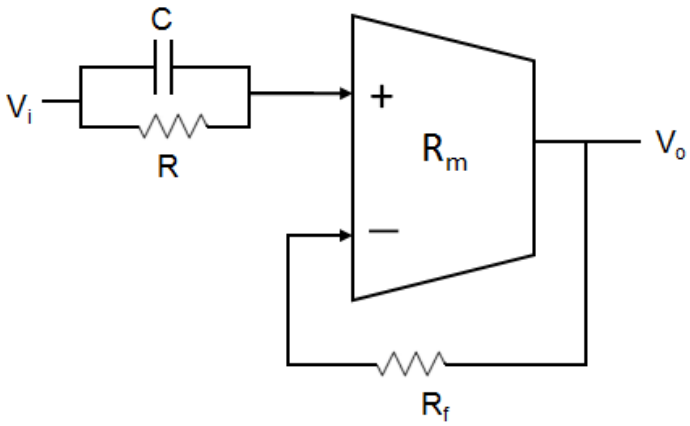

Fig. 3.Proposed PD Controller

These parameters can be electronically tuned by implementing the linear passive resistors using MOS transistors operating in non-saturation region. The resistance value may be adjusted by appropriate choice of gate voltages.

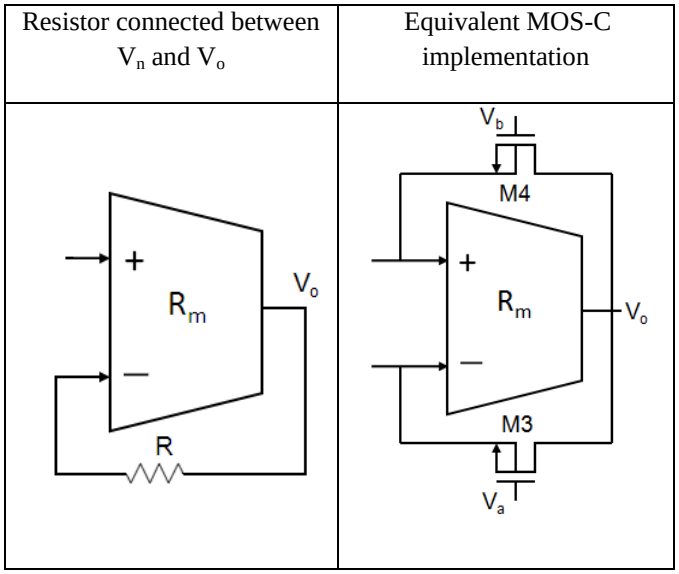

Fig. 4. MOS implementation of a Linear resistance.

The resistors connected to the input terminals of OTRA can easily be implemented using MOS transistors with complete non-linearity cancellation [10]. Fig. 4 shows a typical MOS implementation of resistance connected between negative input and output terminals of OTRA.

The equivalent resistance value is given as

$$R = {}^{1}\Big/_{\mu_n C_{ox}\left({}^{W}\Big/_{L}\right)(V_a - V_b)} \tag{8}$$

where μ_n, C_{ox}, W and L are electron mobility, oxide capacitance per unit gate area, effective channel width, and effective channel length respectively which may be expressed as

$$\mu_n = \frac{\mu_0}{1+\theta(V_{GS}-V_T)} \tag{9}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \tag{10}$$

$$W = W_{drawn} - 2W_D \tag{11}$$

$$L = L_{drawn} - 2L_D \tag{12}$$

Va and Vb are the gate voltages and other symbols have their usual meaning. Fig. 5 shows the MOS-C implementation of the circuit of Fig.3.

3.Non-Ideality Analysis

The non-idealities associated with OTRA based circuits may be divided into two groups. The first group results due to finite trans-resistance gain whereas the second one concerns with the nonzero impedances of p and n terminals of OTRA.

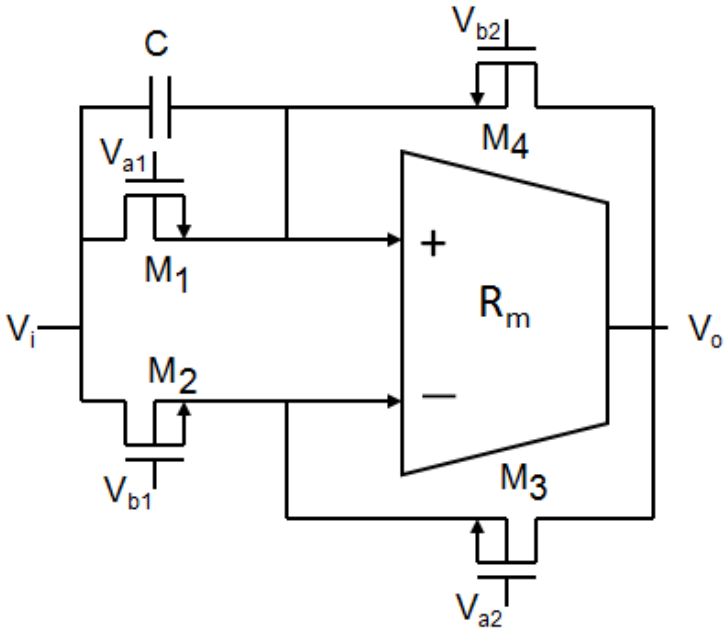

Fig. 5.MOS-C equivalent of Proposed PD Controller

3.1Non- Ideality due to Finite Transresistance Gain

Here the effect of finite trans-resistance gain (R_m) on PD controller is considered and for high frequency applications passive compensation is employed. Ideally the R_m is assumed to approach infinity. However, practically Rm is a frequency dependent finite value. Considering a single pole model for the trans-resistance gain, it can be expressed as

$$R_m = \frac{R_o}{1+{}^{s}/_{\omega_o}} \tag{13}$$

where R_0 is dc transresistance gain.
For high frequency applications the trans-resistance gain, reduces to

$$R_m(s) \approx \frac{1}{sC_p} \quad \text{where} \quad C_p = \frac{1}{R_0\omega_0} \tag{14}$$

Taking this effect into account (6) modifies to

$$\frac{V_o}{V_i} = \frac{R_f}{R(1+sC_pR_f)} + sC\frac{R_f}{1+sC_pR_f} \tag{15}$$

For high-frequency applications, compensation methods must be employed to account for the error introduced in (4). Considering the circuit shown in Fig.6, equation (15) modifies to

$$\frac{V_o}{V_i} = \frac{R_f}{R(1+R_f(sC_p-sY))} + \frac{sCR_f}{1+R_f(sC_p-sY)} \tag{16}$$

By taking Y = C_p, (16) reduces to (6). The effect of R_m can thus be eliminated by connecting a single capacitor between the non inverting terminal and the output as shown in Fig.6, and the passive compensation can be achieved.

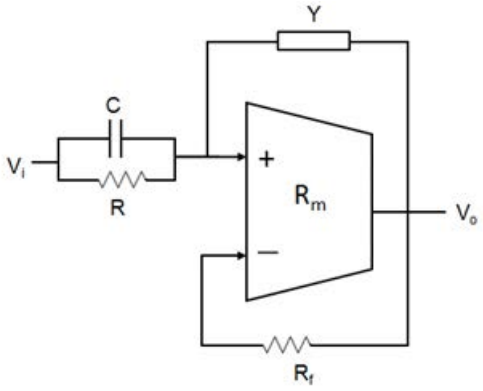

Fig. 6.Compensated PD Controller

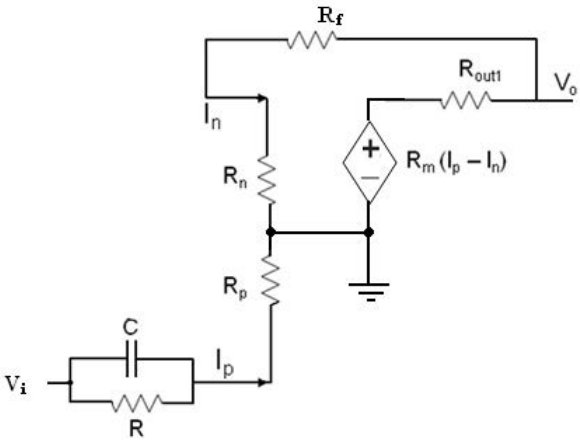

Fig. 7 AC equivalent of proposed PD Controller

3.2 Effect of Nonzero Impedances of p and n Terminals

Ideally input as well as output resistances are assumed to be zero. To consider the effect of and non zero values of input resistances (R_n and R_p) and output resistances (R_{out1}) on proposed PD controller AC equivalent of the controller using AC equivalent of OTRA is drawn and is shown in fig 7.

Routine analysis of Fig. 6(a) results in terminal currents I_p and I_n as

$$I_p = \frac{V_i(1+sCR)}{R+R_p+sCRR_p} \tag{17}$$

$$I_n = \frac{V_o}{R_f+R_n} \tag{18}$$

Thus the output voltage V_o can be written as

$$V_o = R_m(I_p - I_n) - R_{out1}I_n \tag{19}$$

$$V_o = R_m I_p - (R_m + R_{out1})I_n \tag{20}$$

As $R_m >> R_{out1}$ so $R_m + R_{out1} \approx R_m$ and hence

$$V_o \approx R_m(I_p - I_n) \tag{21}$$

Substituting I_p and I_n, (21) results in

$$V_o = R_m\left(\frac{V_i(1+sCR)}{R+R_p+sCRR_p} - \frac{V_o}{R_f+R_n}\right) \tag{22}$$

$$\frac{V_o}{V_i} = \frac{R_m(1+sCR)}{(R+R_p)\left(1+\frac{sCRR_p}{R+R_p}\right)\left(1+\frac{R_m}{R_f+R_n}\right)} \tag{23}$$

As $R >> R_p$, $R_m >> (R_f + R_n)$ and $R_f >> R_n$ and so (23) yields

$$\frac{V_o}{V_i} \approx \frac{R_m(1+sCR)}{R(1+sCR_p)\frac{R_m}{R_f}} \tag{24}$$

$$= \frac{R_f(1+sCR)}{R(1+sCR_p)} \tag{25}$$

Comparing (25) with (6) it is observed a parasitic pole with pole frequency $1/R_pC$ is introduced. The parasitic pole frequency would be much beyond the zero frequency (1/CR) for a selection of $R>>R_p$, and would not influence the performance of the system.

4. Simulation Results

In order to verify the theoretical propositions simulations are performed using PSPICE program. For simulation CMOS implementation of the OTRA proposed in [12] was used. The SPICE simulation was performed using 0.18µm, Level 7, CMOS process parameters provided by MOSIS and supply voltages taken are ±1.5 V. For the proposed controller shown in Fig. 3, the values of passive element are chosen as R = 10KΩ, R_f = 20KΩ and C = 20pF. For time domain analysis, a 3mV peak triangular input voltage is applied. For this input the output of the proposed controller would be given by

$$V_o(t) = \left(\frac{R_f}{R}\right).V_i(t) + CR_f\frac{dV_i(t)}{dt} \tag{26}$$

Both ideal and simulated results are presented in Fig. 8a and are found in agreement with (26). In the magnitude response of the proposed controller given by (3) first term is dominant for low frequencies ($\omega << 1/T_d$) and thus would result in a constant output ($\approx 20 \log K_p$) whereas for high frequencies ($\omega >> 1/T_d$) the second term of the response becomes effective and the output would be represented by a straight line having a slope of 20dB/decade. Similarly for phase response for low frequencies phase would be 0° , at $\omega = 1/T_d$ it would be 45° and would approach 90° for extremely high frequencies. It is observed that the frequency domain response of the proposed controller shown in fig.8b is in close agreement to above discussion.

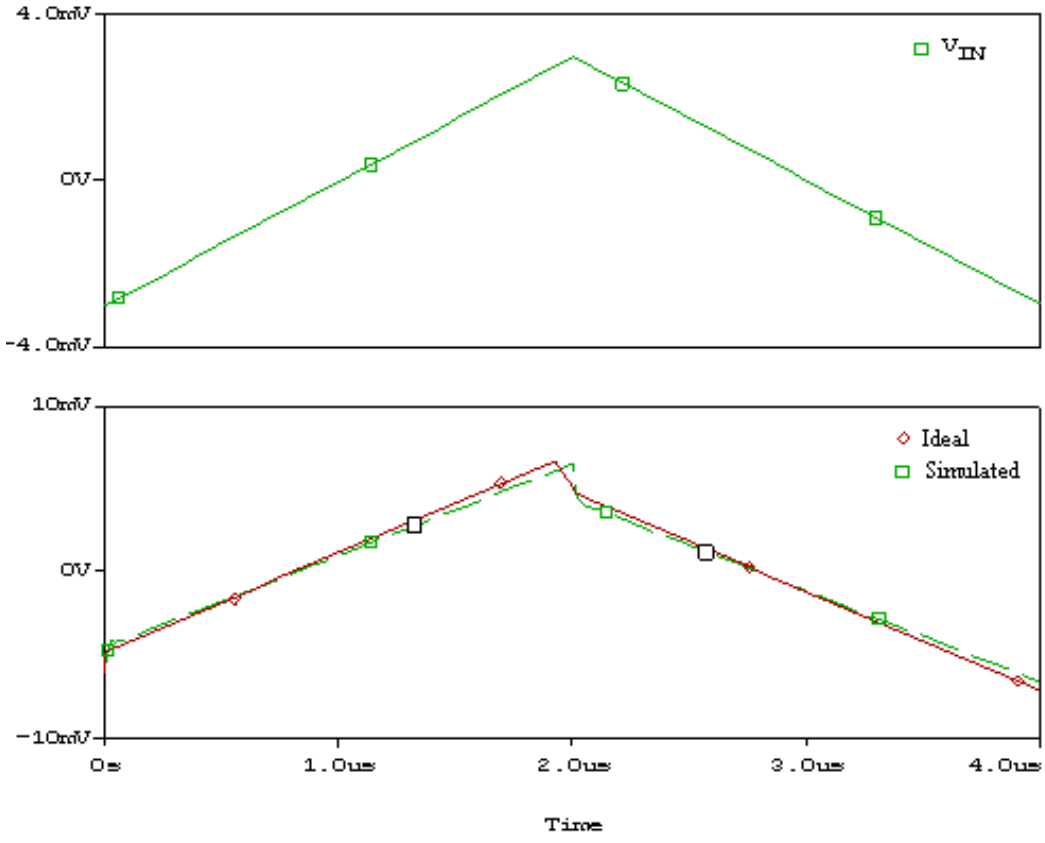

Fig. 8a. Transient response of the PD Controller.

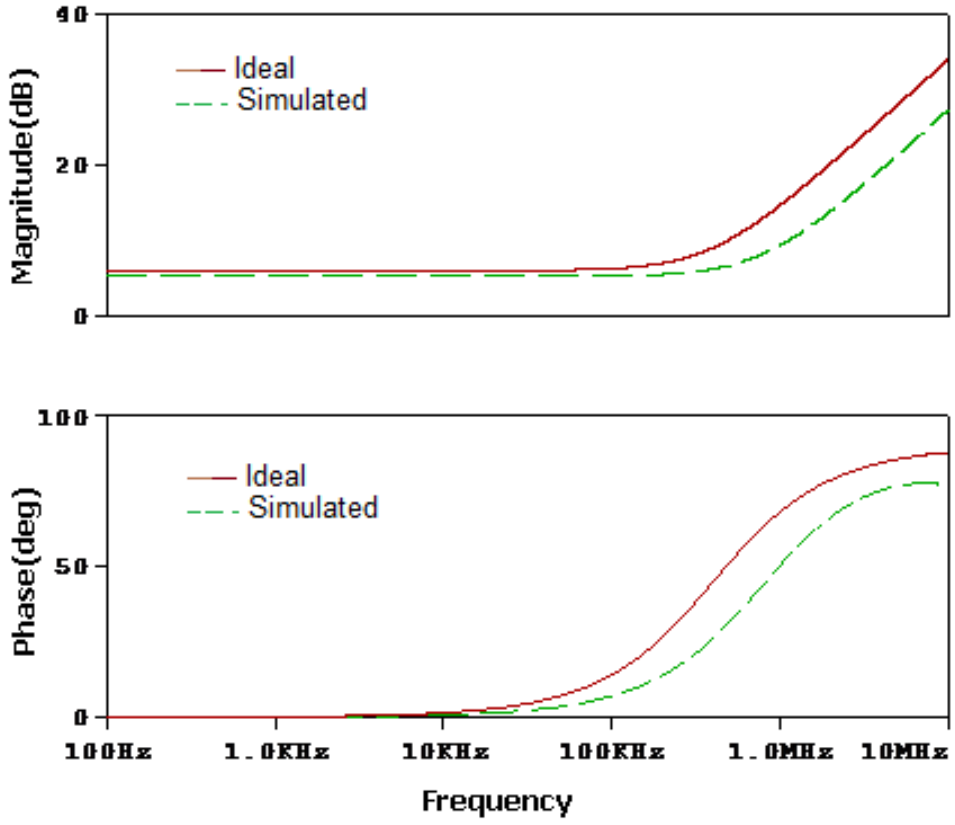

Fig. 8b. Frequency and phase Response of PD controller.

For MOS-C implemented PD controller shown in Fig 5 the aspect ratios of the transistors used for implementing the resistances are listed in Table.1.

Table1.Aspect ratios of transistors used for resistance implementation

Transistor	W(µm)/L(µm)
M1,M2	0.18µ/.54µ
M3,M4	0.18µ/1.08µ

Gate voltages are set as V_{a1}= V_{a2} = 1.2V and Vb1=0.59V, Vb2 =0.64V which result in resistance values as R ≈10KΩ R_f ≈20KΩ and the chosen value of C = 20pF.The ideal and simulated time domain response of MOS-C implemented PD controller, for a 3mV peak triangular input voltage are shown in Fig. 9a. Fig. 9b represents the frequency domain characteristics of the same.

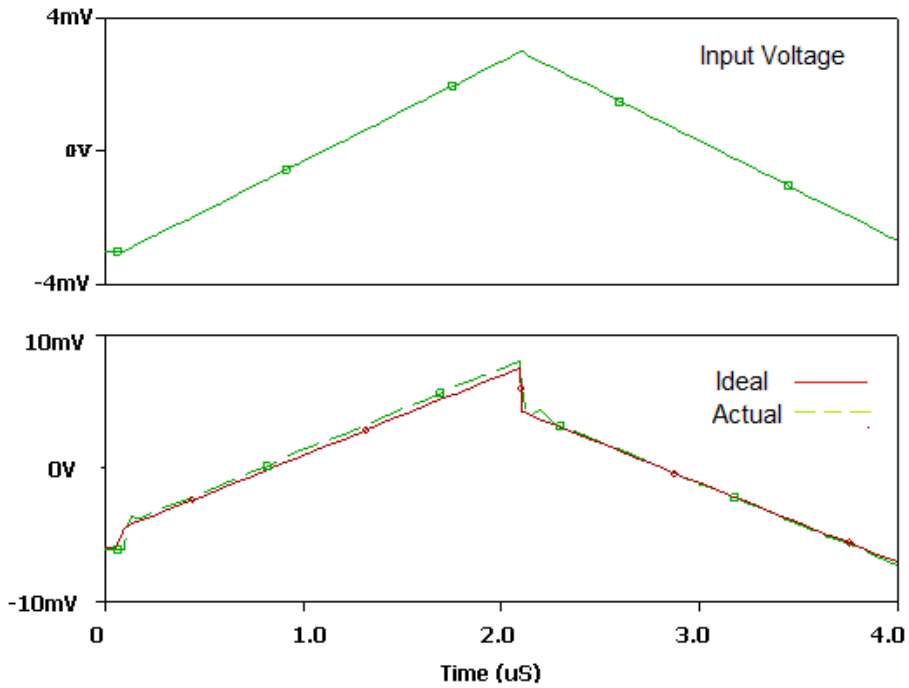

Fig. 9a.Transient response of the MOS-C PD Controller.

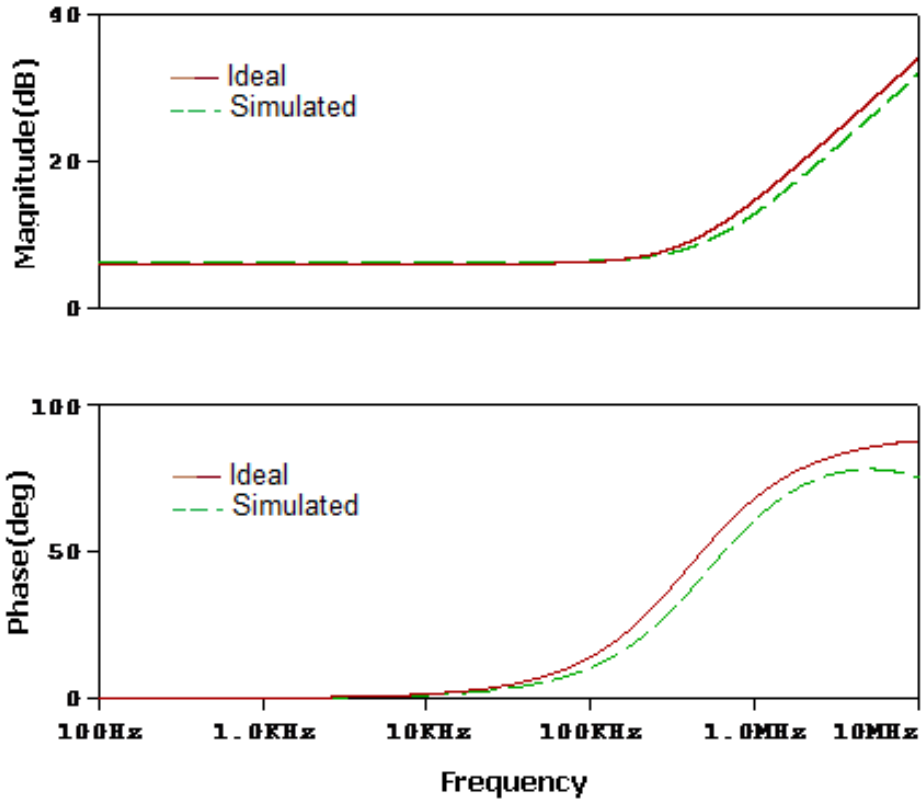

Fig. 9b.Frequency and phase Response of the MOS-C PD Controller.

Fig. 10 shows a closed loop control system realized using the proposed PD controller and a second order low-pass filter (LPF). The LPF is shown in Fig. 11.

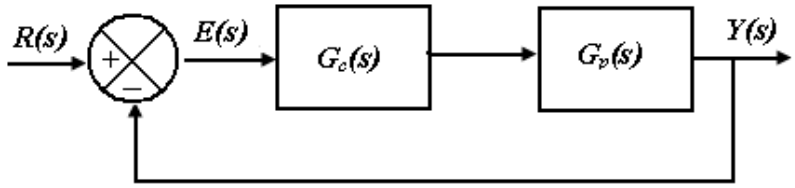

Fig.10.Closed Loop Control System.

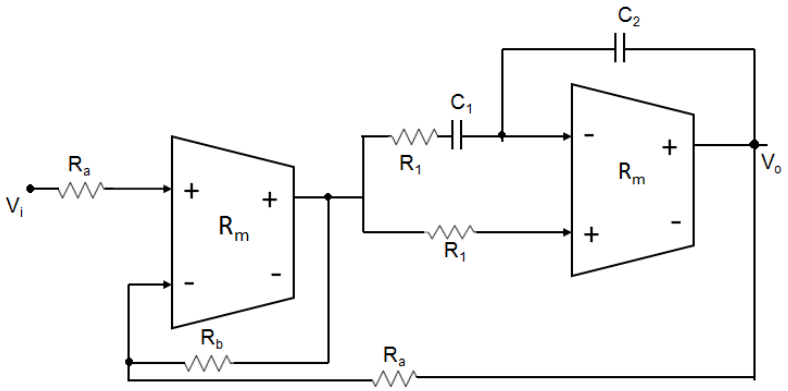

Fig. 11.Second order Low Pass filter.

The transfer function of the LPF is given as

$$\frac{V_0(s)}{V_i(s)} = \frac{G_1{}^2}{s^2C_1C_2+sC_2G_1+KG_1^2} \tag{27}$$

Where $K=R_a/R_b$. The values of passive element for the filters are selected as $R_a=R_b$ =20KΩ, R_1=2KΩ, and $C_1= C_2$=20pF which result in

$$\frac{V_0(s)}{V_i(s)} = \frac{6.25*10^{14}}{s^2+25*10^6s+6.25*10^{14}} \tag{28}$$

Now a PD controller, with the component values R=5K, R_f=15KΩ and C=8pF resulting in K_P=3 and $K_d=0.12\times10^{-6}{}_s$ is added to form control system of Fig. 10.
Fig. 12a shows the step response of the LPF without PD controller for a step input of 50mV whereas Fig.12b depicts the effect of PD controller on step response of the closed loop system.

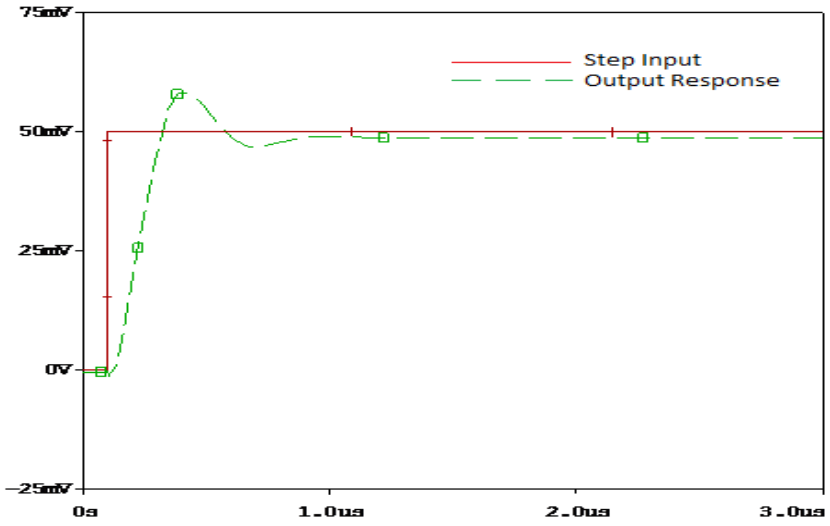

Fig. 12a.Step Response of a second order system without PD controller.

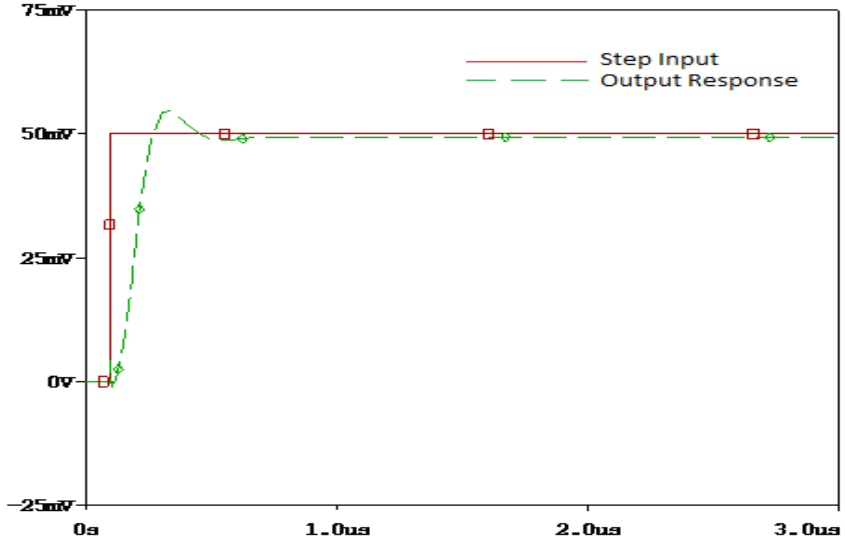

Fig.12b. Step Response of a second order system with PD controller.

Performance comparison of second order system with and without PD controller is shown in Table. 2. It is clearly visible from the table 2 that the response of the system has been improved.

Table. 2. Performance Comparison.

Parameter	Without PD Controller	With PD Controller
Overshoot	19.56%	10.59%
Peak output	58.26mV	54.63mV
Rise time	140.43ns	107.78ns

Conclusion

A single differential Operational transresistance (OTRA) based voltage mode proportional-derivative (PD) controller has been presented which possesses the feature of independent tuning of proportional (Kp) and derivative (Kd) constants. This controller can be made fully integrated by implementing the resistors using MOS transistors operating in linear region. As an application, a second order closed loop system is designed and simulated using SPICE program. The simulated results are in line with the proposed theory.

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